Application Note

CMX7031:
An Example Core Design for a Complete Family Radio

AN/2WR/7031/FRS/3 July 2007

1 Introduction

The CMX7031 is a highly integrated baseband processor that is targeted at analog two way radio applications. Professional and leisure radio designs can benefit from the extensive functionality, low power consumption, and aggressive pricing offered by the CMX7031. Additionally, the ability to enhance its functions through updated Function Image™ files allows the CMX7031 to offer enhanced features for no additional cost.

The purpose of this application note is to illustrate how the CMX7031 can be configured for a feature rich "family radio" product. This document will describe how the CMX7031 can be configured to perform the following functions:

- Half Duplex voice communications
- Text Messaging (both open and private messages)
- GPS location data
- Unique 'ring tones'
- Audible alerting tones, for example indicating when a button has been pressed
- 'All Call' (urgent) call capability
- RF Synthesizer configuration
- System clock configuration

This document reflects the CMX7031 device functionality after being loaded with Function Image 1.3. Use of this document with other Function Images™ may result in undesired operation. Discussion of Function Image™ loading procedures is beyond the scope of this document and is fully discussed in the CMX7031 datasheet.

The following information should be consulted while reviewing this application note:

1. CMX7031 Datasheet
2. CMX7031 User Manual
3. CMX7031 Synthesizer Calculator Application Note and Spreadsheet

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2 CMX7031 Function Image™ 1.3 Feature Set

In addition to being backward compatible with previous Function Images, Function Image™ 1.3 loads the following functions into the CMX7031:

Base configuration

- Single channel half duplex operation
- Three analogue inputs with input amplifier and programmable gain adjustment for connection to microphone and demodulator sections
- Transmit output drivers with programmable level adjustment for single point, two point, and I / Q modulation.
- Flexible Rx input signal routing

Audio processing

- Tx channel filtering for 12.5kHz and 25kHz bandwidths
- Tx signal limiting (software adjustable)
- Rx channel filtering (300Hz HPF and 2.55kHz / 3.0kHz LPF)
- Preemphasis and deemphasis
- Companding
- Scrambling (frequency inversion with adjustable split point)
- Digital gain adjustment
- Audio output with digital gain adjustment
- Selectable order of signal processing blocks

Subaudio signalling

- CTCSS encoder / decoder (preprogrammed with 51 tones, plus user programmable tone)
- DCS encoder / decoder (programmable 23/24 bit)

Inband signalling

- XTCSS encoder/decoder
- Programmable Selcall encoder / decoder
- Programmable audio tone generator (for custom audio tones)
- DTMF encoder

Data modem

- 1200 / 2400 baud FFSK / MSK modem
    - Data packet mode incorporating interleaving, FEC, CRC and data scrambler (functions that are suitable for text messaging / paging, caller identification, caller location, digital poll of remote radio location, GPS information in NMEA 0183 format, general data transfer)
    - Free format mode
- 1200 bps FSK modem for Marine VHF applications

NOAA Weather Radio (for USA and Canada applications)

- WAT detector (Warning Alert Tone, 1050Hz)
- SAME (Specific Area Message Encoding) preamble / end-of-frame detector and data demodulator

Auxiliary

- 2 programmable system clock outputs (384kHz – 20MHz)
- 2 auxiliary ADCs with four selectable input paths
- 4 auxiliary DACs (one with configurable auto ramping profile)
- 2 GPIO pins (can be used as Tx enable and Rx enable signals)

RF

- 2 flexible Integer-N RF synthesizers (100MHz – 600MHz) with phase detectors and charge pumps

3 Description of Scenario

This document will use a combination of a state diagram and pseudocode routines to describe how the CMX7031 can be configured to perform tasks for a possible application. In this "system" we will assume that two hand held FRS radios are being used, both of which are equipped with the CMX7031. The following functions are required:

- Half duplex voice communications
- Text Messaging (both 'open' and 'private' messages)
- GPS location data
- Unique 'ring tones' (single tones and simple melodies)
- 'All Call' (urgent) call capability

Clearly the CMX7031 could be used to implement many more radio designs, however this document is not intended to describe all options but to provide a detailed overview of what is required in software to control the CMX7031.

For engineers who have other requirements and wish to discuss them further or who wish to receive further clarification on the information in this document, please contact the CML Help Desk for your respective geographic area:

North and South America	us.techsupport@cmlmicro.com
China	cn.techsupport@cmlmicro.com
Southeast Asia	sg.techsupport@cmlmicro.com
Europe, Africa, Australia and Asia	techsupport@cmlmicro.com

3.1 Transmit Functions

The FRS radio in this application is configured to transmit on FRS channel 1 (462.5625MHz). The radio user presses the "Push To Talk" (PTT) radio button to begin a voice transmission to the second remote radio. When the PTT button is pressed:

1. If the user has previously configured a "buddy list" in a software look up table, they can scroll through the list and highlight the person(s) they wish to call before pressing the PTT button. This will allow the host microcontroller to reconfigure the CMX7031 for the appropriate Tx channel and CTCSS tone frequency.
2. An audible alerting tone should be generated so the user knows a button was pressed.
3. After the audible alerting tone is generated, the CMX7031 can be used to process the transmitted speech (e.g. preemphasis). The CMX7031 can also generate and transmit a subaudio tone (i.e. CTCSS tone) for remote receiver squelch control.

The user can press the "Poll" button to manually request the location data of the remote user. When the "Poll" button is pressed:

1. An audible alerting tone will be generated by the CMX7031 so the user knows a button was pressed.
2. The CMX7031 will transmit an FFSK / MSK data burst to the remote user. This FFSK / MSK data burst will instruct the remote user to transmit its location data back to the calling radio.

The user can send a text message to a remote user by entering text on the FRS radio and pressing the "Send" button.

1. The user will select the 'text message' function (the activation of the 'text message' function is not described in this document).
2. The user selects the intended recipient of the message and indicates whether the message is 'open' or 'private'.
    - If the user has previously configured a "buddy list", the user can scroll through this list and highlight the desired message recipient(s).

3. The user can compose the text message by one of the two following methods:
    - Preset text messages. The user can scroll through a list of preprogrammed text messages stored on the host microcontroller and highlight the desired message.
    - User typed text messages. The user enters the desired text through the radio's keypad.
4. Once these steps are performed and the "Send" button is pressed, the host microcontroller and CMX7031 can generate an FFSK / MSK data burst containing both the recipient's address and the actual message data.

If a received message has errors, the radio can use its CMX7031 to transmit a "retransmission request" via an FFSK / MSK data burst to the remote radio.

3.2 Receive Functions

In this application, either voice or FFSK / MSK data can be received.

The FRS radio, configured to receive on FRS channel 1 (462.5625MHz), will normally be in "sleep" mode waiting to receive a call. The CMX7031's ADC1 monitors the RSSI signal from the RF transceiver. An incoming transmission will cause the RSSI signal to exceed the ADC's "high" threshold and cause an interrupt to be generated. The host microcontroller should then read the STATUS ($C6) and AUXADC1 DATA ($A9) registers to ensure that the source of the interrupt was a rising RSSI signal. Once the IRQ source has been verified as RSSI, the CMX7031 should be configured for both voice and FFSK / MSK reception.

The next IRQ should indicate the type of incoming call:

- If STATUS ($C6) b11 = 1, CTCSS detection has occurred and a voice call is imminent.
- If STATUS ($C6) b4 = 1, 2400 bps FFSK / MSK has been detected and a data burst is imminent.

If the incoming transmission is a voice call, the CMX7031 will:

- Generate a ring tone to alert the user that a call is about to be heard.
- Process the recovered voice signal for presentation to the external speaker driver.

If the incoming transmission is FFSK / MSK data, the host microcontroller will interpret the received FFSK / MSK message and proceed accordingly.

The user can press the radio's "Monitor" button to listen for all activity on a channel. When this happens:

1. An audible alerting tone will be generated by the CMX7031 so the user knows a button was pressed.
2. The CMX7031 will activate its audio output amplifier to allow any received signal to be passed to the radio's speaker or headset.

3.3 Assumptions

The following assumptions were used in the development of this application note:

- V_{DD} = 3.3V provided by three "AAA" batteries (3 cells x 1.5V / cell = 4.5V nominal).
  - Low dropout regulator used to step down battery voltage for CMX7031.
  - "Low Battery Warning" at 3.6V (arbitrarily chosen).
  - Battery voltage scaled (60% reduction) prior to presentation to CMX7031 AUXADC4 input pin.
- FRS service with 25kHz channel spacing.
- External components configured in accordance with CMX7031 datasheet.
- 19.2MHz TCXO supplies signals to both XTAL / CLK pin and RF CLOCK input (common to both synthesizers). Baseband and RF clocks are derived from this 19.2MHz TCXO input.
- System Clock Generators
  - Clock Output 1 = 12.288MHz
  - Clock Output 2 = 16.384MHz
- Single point modulation used.
- Voice and CTCSS subaudio tone transmitted on MOD1.
  - Voice + CTCSS output level = 500mV$_{RMS}$
    - Voice = 455mV$_{RMS}$
    - CTCSS = 45mV$_{RMS}$
  - **Note:** Actual voice and subaudio tone levels depend on VCO sensitivity and desired deviation; these specifications are application dependent. A discussion of CMX7031 maximum signal levels is presented later in the document.
- Voice:
  - Preemphasis and deemphasis enabled
  - Companding enabled
  - Soft Limiter threshold = 525mV$_{RMS}$
- Subaudio Tones:
  - CTCSS subaudio tone is used during voice transmissions for squelch control.
    - Tone # 20 (131.8Hz) generated during voice transmission.
    - Tone # 1 (67.0Hz) detected during voice reception.
  - No subaudio inversion.
- FFSK / MSK:
  - Transmitted on MOD1 (no subaudio tone used for FFSK / MSK transmissions).
    - MOD1 output level = 500mV$_{RMS}$
  - FFSK / MSK Address = 79 (arbitrarily chosen).
  - 2400 bps, Type 5 message format.
  - Frame length = 80 bytes (arbitrarily chosen).
  - Standard scrambling seed.
  - Default bit sync (0x5555) and frame sync (0xCB23) patterns are used
- Ring Tone
  - 1250Hz ring tone is used in this scenario but the user can select different ring tones or combinations of tones.
  - Ring tone level = 500mV$_{RMS}$
- RSSI signal monitored with ADC1 via AUXADC1 pin during sleep and Rx modes.
  - High threshold (good carrier signal) = 1.85V for –60dBm received signal strength.
  - Low threshold (indicates weak signal) = 0.9V for –100dBm received signal strength.
    Note: The received signal strength values used for this document include no "noise margin". The user must evaluate their application and determine the optimal RSSI threshold and hysteresis settings.
- RF discriminator output is applied to CMX7031 DISC pin.
- CMX7031 AUDIOOUT pin delivers ring / alerting tones and recovered voice to an external speaker driver amplifier for presentation to the radio speaker.
- RF Synthesizer
  - FRS Channel 1 = 462.5625MHz, used for Tx and Rx.
  - CMX7031 Channel 1 Synthesizer used for Tx RF upconversion.
  - CMX7031 Channel 2 Synthesizer used for Rx downconversion.

- ADC (CMX7031 input pin names provided)
  - AUXADC1: RSSI
  - AUXADC2: Tx power amplifier temperature sensor input
  - AUXADC3: TCXO temperature sensor input
  - AUXADC4: Battery voltage
- DAC (CMX7031 output pin names provided)
  - AUXDAC1: Tx power amplifier (ramp up / down profile)
    - RAMDAC feature is used to take advantage of preprogrammed ramp profile.
  - AUXDAC2: Tx power amplifier temperature compensation control voltage
  - AUXDAC3: TCXO temperature compensation control voltage
  - AUXDAC4: Not used

The normal operating mode for the CMX7031 in this application is powered down, monitoring RSSI with ADC1 (STATE 3 from Figure 6).

3.4 Block Diagram

The following figure illustrates the CMX7031 and its interconnections as described in this application note:

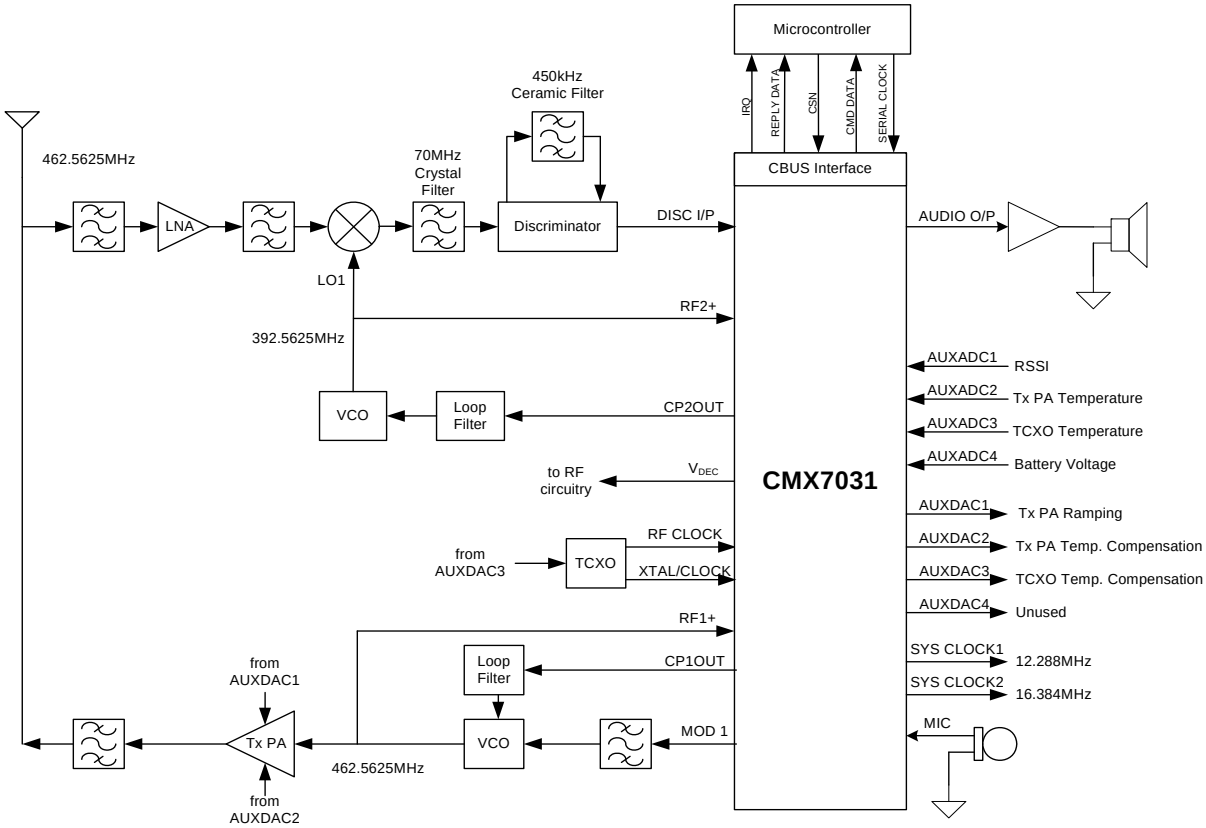

Figure 1: Application Scenario Block Diagram

4 CMX7031 Functional Considerations

4.1 RF Considerations

The CMX7031 includes two RF synthesizers that can be used to minimize external parts count and BOM cost. These synthesizers are referred to as "Channel 1" and "Channel 2" in the CMX7031 documentation. While many different implementations are possible, the following scenario is used in this document:

- Channel 1 Synthesizer
  - Transmit mode, creates 462.5625MHz for FRS channel #1
- Channel 2 Synthesizer
  - Receive mode, creates 392.5625MHz for LO1 (for RF downconversion of FRS channel #1)

Once the desired frequencies are known, the "N" and "R" values for each synthesizer must be calculated. CML has created a spreadsheet, "CMX7031 Synthesizer Calculator", that can quickly calculate N and R values for various requirements. This spreadsheet was used for the N and R register calculations provided in this document. The "CMX7031 Synthesizer Calculator" application note is available upon request.

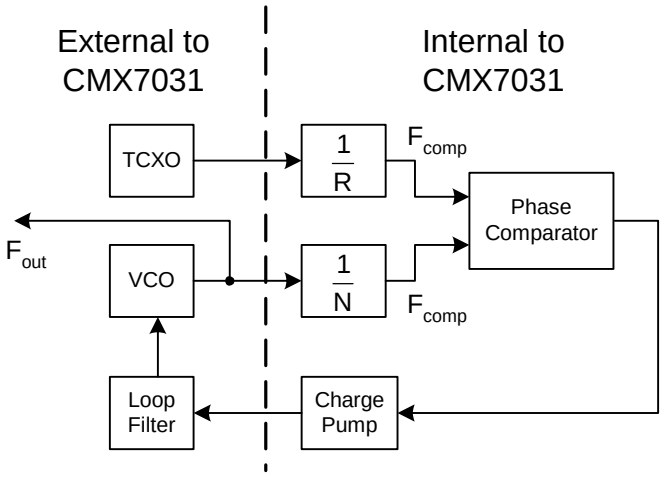

Figure 2: CMX7031 Synthesizer Block Diagram

The comparison frequency, F_{comp}, was chosen to be 12.5kHz so an integer multiple relationship with FRS channel frequencies could be achieved. (FRS channel spacing is 25kHz.) The following table illustrates the register values needed to configure the CMX7031 Channel 1 Synthesizer to transmit on FRS Channel 1.

Synthesized Frequency	Register	Contents
462.5625MHz (FRS Channel 1, Transmit)	Tx N b9..0	0x408D
	Tx N b19..0	0x4424
	Tx R b9..0	0x4A00
	Tx R b12..0	0x4C01

Table 1: RF Channel Data ($B2) Settings for Channel 1 Synthesizer

The second synthesizer in the CMX7031 is used to generate LO1 signal for the RF to IF1 downconversion. The following table illustrates the register values needed to configure the CMX7031 Channel 2 Synthesizer to generate this LO frequency:

Required LO1 Frequency	Register	Contents
392.5625MHz (FRS Channel #1)	Rx N b9..0	0x72AD
	Rx N b19..0	0x741E
	Rx R b9..0	0x7A00
	Rx R b12..0	0x7C01

Table 2: RF Channel Data ($B2) Settings for Channel 2 Synthesizer

Channel 1 and Channel 2 Synthesizers each have "Tx" and "Rx" sections, but there is no requirement that the "Tx" section actually be used for transmit operation. Bits 10..9 and 2..1 of RF Channel Control ($B3) register determine which synthesizer settings (Tx or Rx) are enabled. The user is free to select the channel and section for their particular application regardless of whether the device is in transmit or receive mode.

4.2 ADC Considerations

The CMX7031 provides two 10-bit ADCs that are multiplexed between four different inputs. In this application, the ADC inputs are used as follows:

- AUXADC1: RSSI
- AUXADC2: Input from Tx power amplifier temperature sensor
- AUXADC3: Input from TCXO temperature sensor
- AUXADC4: Battery voltage

In an actual application it would likely not be necessary to continuously monitor all four of these parameters. For example, RSSI would not require monitoring during Tx mode, and Tx PA temperature would not require monitoring during Rx mode. The host microcontroller can switch the ADC multiplexer inputs to allow periodic monitoring of these parameters as necessary. This level of control is application specific, however, and is therefore not discussed in this document.

The bit resolution of the ADCs in this application is:

$$\frac{V_{DD}}{(2^{10}-1)} = \frac{3.3V}{1023} = \frac{3.23mV}{bit}$$

The ADC input level range is 10% to 90% of V_{DD}, which translates from 0.33V to 2.97V in this application.

Rolling averaging is used with the CMX7031 ADCs in this application. With this averaging method, a fraction of the current ADC input value will be added to the previously calculated ADC reading. Programming register blocks P3.0 (ADC1) and P3.1 (ADC2) determine the scaling factors for the current and previous ADC values; the values stored in these registers can vary from 0 to 8.

P3.0 or P3.1 Value	Current Value Scale Factor	Previous Value Scale Factor
0	0.5	0.5
1	0.25	0.75
2	0.125	0.875
3	0.0625	0.9375
4	0.03125	0.96875
5	0.015625	0.984375
6	0.007813	0.992188
7	0.003906	0.996094
8	0.001953	0.998047

Table 3: ADC 'Rolling Averaging' Factors

For example, the default values for P3.0 and P3.1 are zero, and this corresponds to a 50% scaling factor applied to each term:

(Current ADC Input x 0.5) + (Previous ADC Value x 0.5) = New ADC Reading

A value of 2 in P3.0 or P3.1 would result in:

(Current ADC Input x 0.125) + (Previous ADC Value x 0.875) = New ADC Reading

The chosen averaging value will directly impact the length of time required to achieve an accurate reading. The following table illustrates the number of samples required to achieve 1% accuracy after a large change of ADC input signal (e.g. 100% change). Smaller input signal changes will result in faster convergence:

P3.0 or P3.1 Value	Required # of samples to achieve <1% error	Time required to achieve <1% error (ms)
0	7	0.44
1	17	1.06
2	35	2.19
3	72	4.50
4	146	9.13
5	293	18.31
6	588	36.75
7	1177	73.56
8	2356	147.25

Table 4: Impact of ADC Averaging Lengths for Large Input Signal Changes

A tradeoff exists between response time and noise immunity, and the optimal averaging setting is application dependent.

This application scenario monitors battery voltage so that the host microcontroller can be alerted to a weak battery condition. The battery voltage will normally exceed the CMX7031 V_{DD} of 3.3V, so the

battery voltage must be scaled prior to application to the CMX7031 ADC. Such signal scaling is application dependent and is not discussed in this document. For the purposes of this document, the battery voltage applied to the CMX7031 ADC is 40% of its actual value. For example, a low battery condition of 3.6V is presented to AUXADC 2 input pin as 1.44V.

4.3 DAC Considerations

Three of the four CMX7031 DACs are used in this application (CMX7031 DAC output pin names are provided):

- AUX DAC 1: Tx power amplifier power ramping control signal.
- AUX DAC 2: Tx power amplifier temperature compensation signal.
- AUX DAC 3: TCXO temperature compensation signal.

The host microcontroller writes digital data to the AuxDAC Control / Data ($A8) register to create control signals for external devices. The bit resolution of the DACs in this application is:

$$\frac{V_{DD}}{(2^{10}-1)} = \frac{3.3V}{1023} = \frac{3.23mV}{bit}$$

The DAC output level range is 10% to 90% of V_{DD}, which translates from 0.33V to 2.97V in this application. An example calculation for a desired 1.2V DAC output level is as follows:

$$\frac{1.2V}{3.23mV/bit} \cong 372d = 0x174$$

A value of 0x174 should be loaded into $A8 b9..0 to create a 1.2V DAC output level.

DAC 1 can be used as a typical DAC or as a RAMDAC. A preprogrammed set of ramping values (corresponding to a raised cosine response) can be used for RAMDAC operation, or custom values can be loaded into Programming Register blocks P3.11 – P3.75 if desired. RAMDAC operation is activated with $A8 b12 = 1, and the scan rate (ramping rate) is determined with b5..3 of $A8.

The DAC 1 is used as a RAMDAC with preprogrammed ramping profile in this project.

4.4 System Clock Generator Considerations

The CMX7031 can supply two clock signals, in the range of 384kHz to 20.0MHz, for use by external devices. This feature can reduce external parts count and BOM cost.

The configuration process for the system clock generators is straightforward.

- Select the desired output frequency and clock generator.
- Select a reference divider ratio to create a reference clock frequency that is integer divisible by the desired output frequency.
- Select a PLL division ratio that reduces the VCO output frequency to the reference clock frequency. The system clock PLL VCO frequency must be at least double the desired output frequency. The PLL division ratio helps determine the VCO frequency. In other words, the product of the division ratio and the reference clock frequency should yield a VCO frequency which is integer divisible by the final output frequency.
- Select the VCO output division ratio to create the desired output frequency.

The following figure illustrates this process:

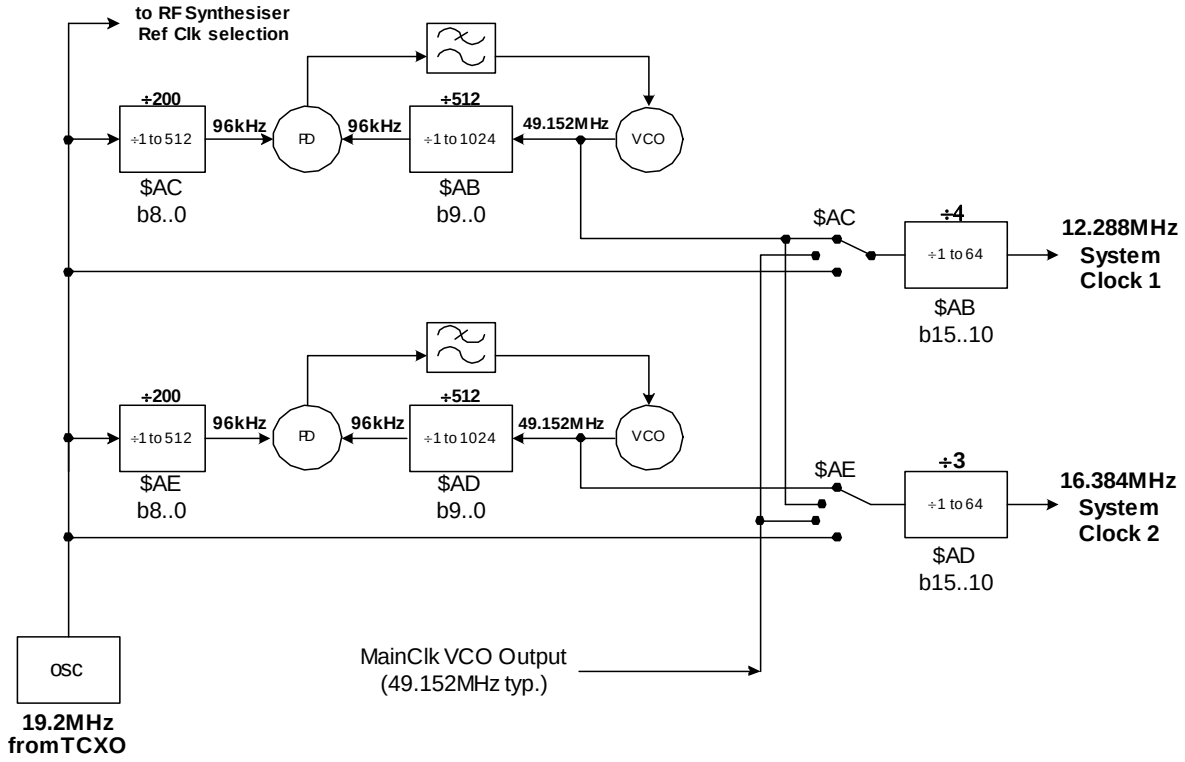

Figure 3: Example Configuration for System Clock Generators

Register	Contents	Comments
$AB System Clk 1 PLL	0x1200	SysClk1 VCO output divider = 4, SysClk1 PLL divider = 512
$AC System Clk 1 Ref	0xE0C8	SysClk1 source = SysClk1 PLL, SysClk1 PLL enabled, normal O / P slew, reference divider = 200.
$AD System Clk 2 PLL	0x0E00	SysClk2 VCO output divider = 3, SysClk2 PLL divider = 512
$AE System Clk 2 Ref	0xE0C8	SysClk2 source = SysClk2 PLL, SysClk2 PLL enabled, normal O / P slew, reference divider = 200.

Table 5: Example Settings for System Clock Generators

This example application uses an external 19.2MHz TCXO to derive the system clock outputs and the CMX7031 main clock signal. Since the external TCXO frequency is not the default 6.144MHz value, adjustments to Programming Register blocks P3.2 through P3.7 are required to ensure proper operation. These adjustments are described in the section for STATE 2, Setup.

The CBUS registers $BC and $BD (for "MainClk" derivation) are controlled automatically by the Function Image™ and must not be accessed by the user. Please consult Section 6.13.2 of the CMX7031 data sheet for more information.

4.5 FFSK / MSK Considerations

The FCC modified the rules concerning FRS radios and data transmission. The key points of these rule changes include:

- Brief text (data) messages can now be transmitted.
- A data transmission cannot be longer than 1 second.
- A radio cannot transmit data more often than once each 30 seconds, but an exception is made to allow the radio to autonomously transmit its location data when polled to do so by another radio.

Data transmission at the fastest possible rate is desired in order to maximize the opportunity provided by these rule changes. Since FRS radios have limited bandwidth, and since the data must be suitable for "voice path" transmission and reception, 2400bps is the optimal tradeoff between transmission speed and occupied bandwidth.

The CMX7031 offers six different FFSK / MSK data formats that differ in error detection, error correction, and robustness to burst errors. The CMX7031's most robust FFSK / MSK message format, "Type 5", provides maximum protection against errors and has been selected for this application.

Since the time available for transmission is limited, the amount of data available for transfer should be considered. The following table lists the 'overhead' requirements for the Type 5 message format and the amount of actual data available for transfer in one second.

Maximum bits in 1 second	2400
Frame Head length in bits (includes 4bits FEC for each Control Field byte)	80
Length of final CRC, in bits (assumes > 16 bytes of user data)	32
Available bits remaining in 1 second	2288
Length of each data byte + FEC, in bits	12
Available bits / (data byte + FEC), in bytes	190.7
Estimated # of user data bytes	190
Estimated time for {Frame Head + User Data + Final CRC}, seconds	0.99667

Table 6: Estimation of Data Throughput for Type 5 Message Format

Each 8-bit character has 4 bits of FEC automatically added by the CMX7031 in Type 5 message format. As can be seen from the table, 190 8-bit characters can be transmitted in one second using the robust Type 5 message format. This amount of data can easily convey multiple short sentences or phrases, and this is exactly the type of information typically communicated via text messaging.

The Type 5 message format utilizes a “frame head” that contains address and control information. The Frame Head contents are listed in the following table:

Frame Head Byte	Comments
Bit Sync	Value is loaded into PROGRAMMING Register blocks P0.8 and P0.9. Default value after C-BUS reset or power on reset is 0x5555.
Frame Sync	Value is loaded into PROGRAMMING Register blocks P0.0 through P0.3. Default value after C-BUS reset or power on reset is 0xCB23.
Address Byte	User defined value is loaded into TX DATA Register ($CA), b15..8. Range of valid address is 1-255 (decimal).
Format Byte	Automatically generated by the CMX7031; value depends on b7..5 of MODEM CONTROL ($C7) Register.
Size / Information Byte	User defined, value is loaded into TX DATA Register ($CA), b7..0. Range of valid sizes is 1-255 (decimal).
Checksum A	Automatically generated by the CMX7031.

Table 7: FFSK / MSK Type 5 Message Format Frame Head Contents

4.6 Transmit Signal Level Considerations

For V_{DD} = 3.3V, the maximum output level from the CMX7031 is:

- Maximum level = AV_{DD} - 0.5V = 3.3V - 0.5V = 2.8V
- Minimum level = 0.5V
- Peak to peak signal = max - min = 2.8V - 0.5V = 2.3 V_{PP} = 813mV_{RMS} (centered around V_{DD} / 2)

The assumptions for Tx audio levels for this application are:

- Voice + CTCSS = 500 mV_{RMS}
  - Voice = 455mV_{RMS}
  - CTCSS = 45mV_{RMS}
- Soft Limiter threshold = 525mV_{RMS}

4.6.1 Transmit Audio Path Considerations

Working backward through the signal path allows determination of the optimum input signal level. (Note: For this example, the MOD1 attenuator and Fine Output Gain 1 is set to 0dB.)

In a typical application, the CTCSS transmit level is 20dB lower than the voice signal. Since the sum of the voice signal and CTCSS tone are desired to be 500mV_{RMS}, the maximum voice signal output from the soft limiter is 455mV_{RMS}, and the CTCSS tone level is 45mV_{RMS}.

The preemphasis block boosts the amplitude of higher input frequencies (e.g. 3kHz) by a factor of three as compared to low input frequencies (e.g. 1kHz). Consequently, the preemphasis input signal must be 455 ÷ 3 ≅ 152mV_{RMS}.

The compressor has a 2:1 characteristic; a 2dB increase in input signal results in a 1dB output signal increase. The “knee” of the compression response is 100mV_{RMS}. Since the compressor output level is known, the compressor input can be derived:

- Output Level, in dB, referenced to 100mV_{RMS}: 20 log (152 / 100) = 3.6dB
- Input Level in dB = 2 x Output Level in dB = 3.6dB x 2 ≅ 7.3dB
- Input Level, referenced to 100mV_{RMS}: 7.3dB = 20 log (x / 100) ∴ x = 231mV_{RMS}

The Input 1 or Input 2 gain stages can provide from 0dB to 22.4dB of gain. (Gain settings are adjusted in the Input Gain and Output Signal Routing ($B1) register.) For the purposes of this example, the external components surrounding the CMX7031 input amplifier are configured for unity gain. Therefore, the input level for the Input 1 or 2 internal amplifier is as follows:

- If Input 1 or 2 gain = 0dB, the input to Input 1 or 2 amplifier = 231mV$_{RMS}$.
- If Input 1 or 2 gain = 22.4dB, the input to Input 1 or 2 amplifier ≅ 18mV$_{RMS}$.

The gain stages, both internal and external, can be adjusted for various input signals so long as these figures are not exceeded. The following figure illustrates the transmit signal path with the previously calculated signal levels:

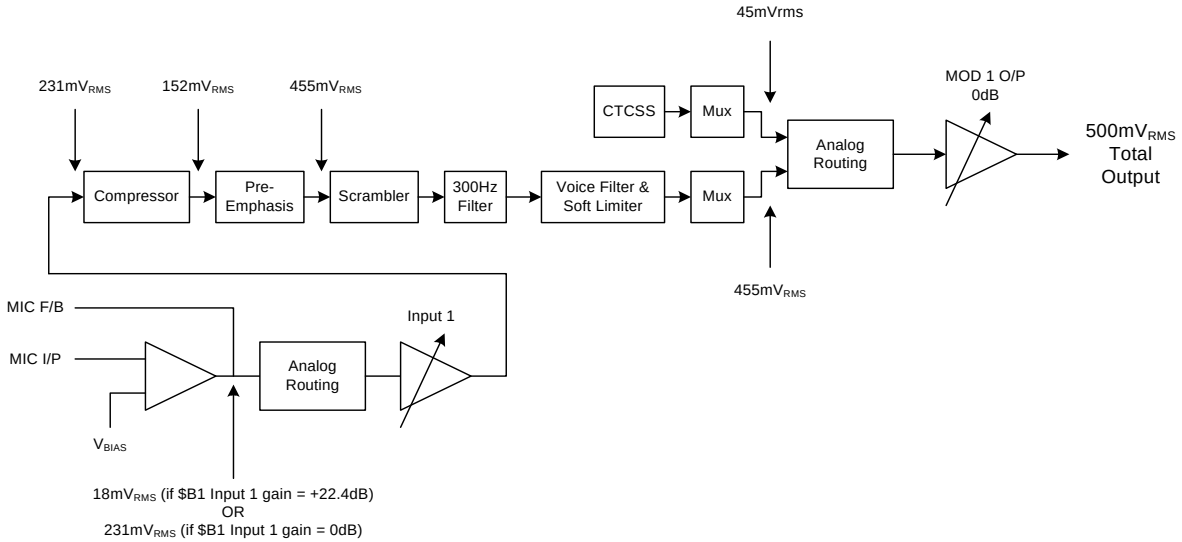

Figure 4: Transmit Audio Signal Level Example (with preferred signal processing path)

4.6.2 Tx Limiter Calculations

The Tx soft limiter threshold (centered on AV$_{DD}$ / 2) is determined by the value loaded into Programming Block P4.7. The programmed value required for 525mV$_{RMS}$ limiting can be determined as follows:

Bit resolution = AV$_{DD}$ / 16384 = 3.3V / 16384 = 201μV / bit

Desired limiting threshold = 525mV$_{RMS}$ = 1.48V$_{PP}$

Number of bits for desired limiting threshold = 1.48 V$_{PP}$ / (201μV / bit) ≅ 7348 bits

7348d = 0x1CB4

Since the two uppermost bits of P4.7 are zeros, a value of 0x1CB4 loaded into P4.7 will cause Tx limiting to occur at 525mV$_{RMS}$ signal level, centered on AV$_{DD}$ / 2.

4.6.3 CTCSS Tone Transmit Calculations

The CTCSS tone transmit level is determined by the value loaded into Programming Block P2.0. The programmed value corresponding to $45mV_{RMS}$ can be determined as follows:

Bit resolution = AV_{DD} / 16384 = 3.3V / 16384 = 201μV / bit

Desired tone level = $45mV_{RMS}$ = $127.3mV_{PP}$

Number of bits for desired level = $127.3mV_{PP}$ / (201μV / bit) = 632 bits

632d = 0x278

The resulting value to be programmed into P2.0 is 0xE278.

4.6.4 MSK and Inband Tone Transmit Signal Calculations

The MSK and Inband tone transmit level is determined by the value loaded into Programming Block P1.0. The programmed value corresponding to $500mV_{RMS}$ can be determined as follows:

Bit resolution = AV_{DD} / 2048 = 3.3V / 2048 = 1.6mV / bit

Desired tone level = $500mV_{RMS}$ = $1.41V_{PP}$

Number of bits for desired level = $1.41V_{PP}$ / (1.6mV / bit) ≅ 875 bits

875d = 0x36B

With P1.0 b0 = 0, the resulting value for P1.0 is 0xD6D6.

4.7 Receive Signal Level Considerations

The CMX7031 audio output driver has a minimum load resistance rating of 20kΩ, so an external speaker driver will be required.

For V_{DD} = 3.3V, the maximum audio output level from the CMX7031 is:

- Maximum level = AV_{DD} - 0.5V = 3.3V - 0.5V = 2.8V
- Minimum level = 0.5V
- Peak to peak signal = max - min = 2.8V - 0.5V = $2.3V_{PP}$ = $813mV_{RMS}$ (centered around V_{DD} / 2)

4.7.1 Receive Audio Path Considerations

Working backward through the signal path allows determination of the optimum input signal level. (Note: For this example, the Audio Output attenuator is set to 0dB.)

There is no CTCSS signal to be summed with the audio output; therefore, the output from the expander block is $813mV_{RMS}$.

The expander has a 1:2 characteristic; a 1dB increase in input signal results in a 2dB output signal increase. The “knee” of the expansion response is $100mV_{RMS}$. Since the expander output level is known, the expander input can be derived:

- Output Level, in dB, referenced to $100mV_{RMS}$: 20 log (707 / 100) = 18.2dB
- Input Level in dB = Output Level in dB / 2 = 18.2dB / 2 = 9.1dB
- Input Level, referenced to $100mV_{RMS}$: 9.1dB = 20 log (x / 100) ∴ x = $285mV_{RMS}$

The de-emphasis block boosts the amplitude of lower input frequencies (e.g. 1kHz) by a factor of 3.33 as compared to higher input frequencies (e.g. 3kHz). Consequently, the de-emphasis input signal is $285mV_{RMS}$ / 3.33 ≅ $86mV_{RMS}$.

The Input 1 or Input 2 gain stages can provide from 0dB to 22.4dB of gain. (Gain settings are adjusted in the Input Gain and Output Signal Routing ($B1) register.) For the purposes of this example, the external components surrounding the CMX7031 input amplifier are configured for unity gain. Therefore, the input level for either Input 1 or 2 internal amplifier is as follows:

- If Input 1 or 2 gain = 0dB, the input to Input 1 or 2 amplifier = 86mV$_{RMS}$.
- If Input 1 or 2 gain = 22.4dB, the input to Input 1 or 2 amplifier ≅ 7mV$_{RMS}$.

The gain stages, both internal and external, can be adjusted for various input signals so long as these figures are not exceeded. The following figure illustrates the transmit signal path with maximum signal levels for V_{DD} = 3.3V:

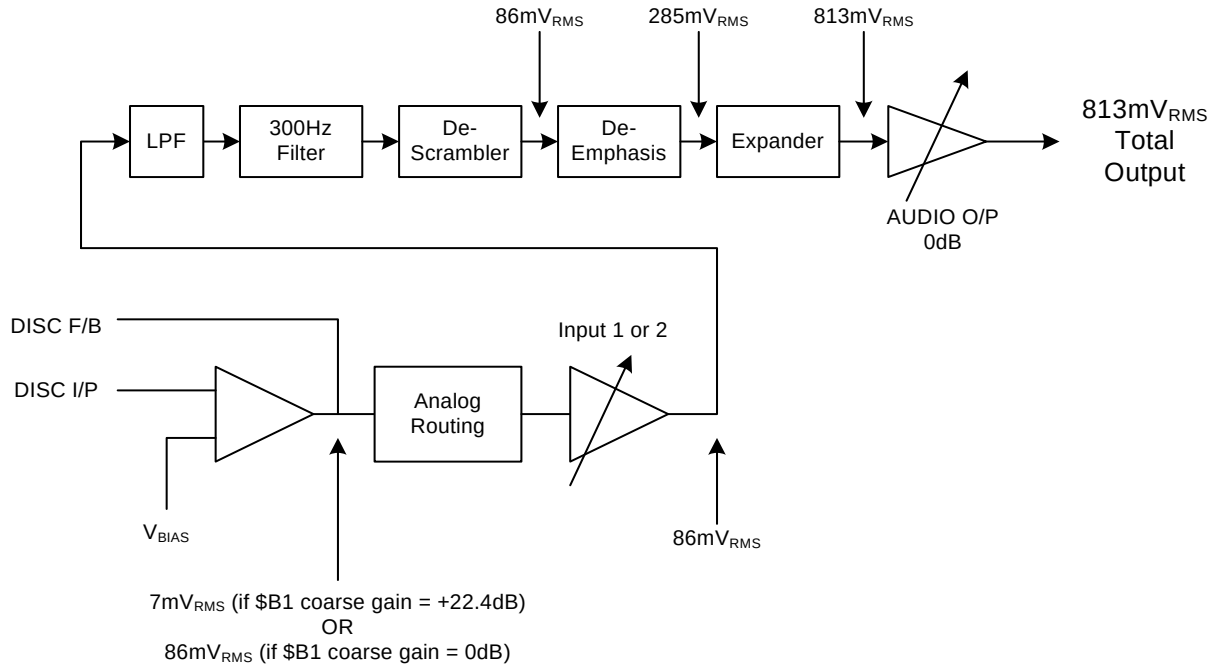

Figure 5: Receive Audio Signal Level Example
(with preferred signal processing path, Vdd = 3.3V)

4.7.2 CTCSS Signal Detection Threshold Calculations

The CTCSS tone detection threshold level is determined by the value loaded into Programming Block P2.1. The programmed value corresponding to 25mV$_{RMS}$ can be determined as follows:

Bit resolution = 2.2mV$_{RMS}$ / bit (at V_{DD} = 3.3V)

Desired CTCSS threshold level = 25mV$_{RMS}$

Number of bits for desired threshold level = 25mV$_{RMS}$ / (2.2mV$_{RMS}$ / bit) ≅ 11 bits

11d = 0xB

The value of 0xB is then loaded into b9..4 of P2.1.

4.7.3 MSK and Inband Signal Detection Threshold Calculations

The MSK and Inband tone detection threshold level is determined by the value loaded into Programming Block P1.1. The programmed value corresponding to $50mV_{RMS}$ (MSK threshold) can be determined as follows:

Bit resolution = $3.99mV_{RMS}$ / bit (at V_{DD} = 3.3V)

Desired threshold level = $50mV_{RMS}$

Number of bits for desired threshold level = $50mV_{RMS}$ / ($3.99mV_{RMS}$ / bit) ≅ 13 bits

13d = 0xD

The value of 0xD is then loaded into b9..4 of P1.1.

5 Operating States

There are several possible operating states for the CMX7031 in this application. The following state flow diagram illustrates the possible transitions between the various operating states.

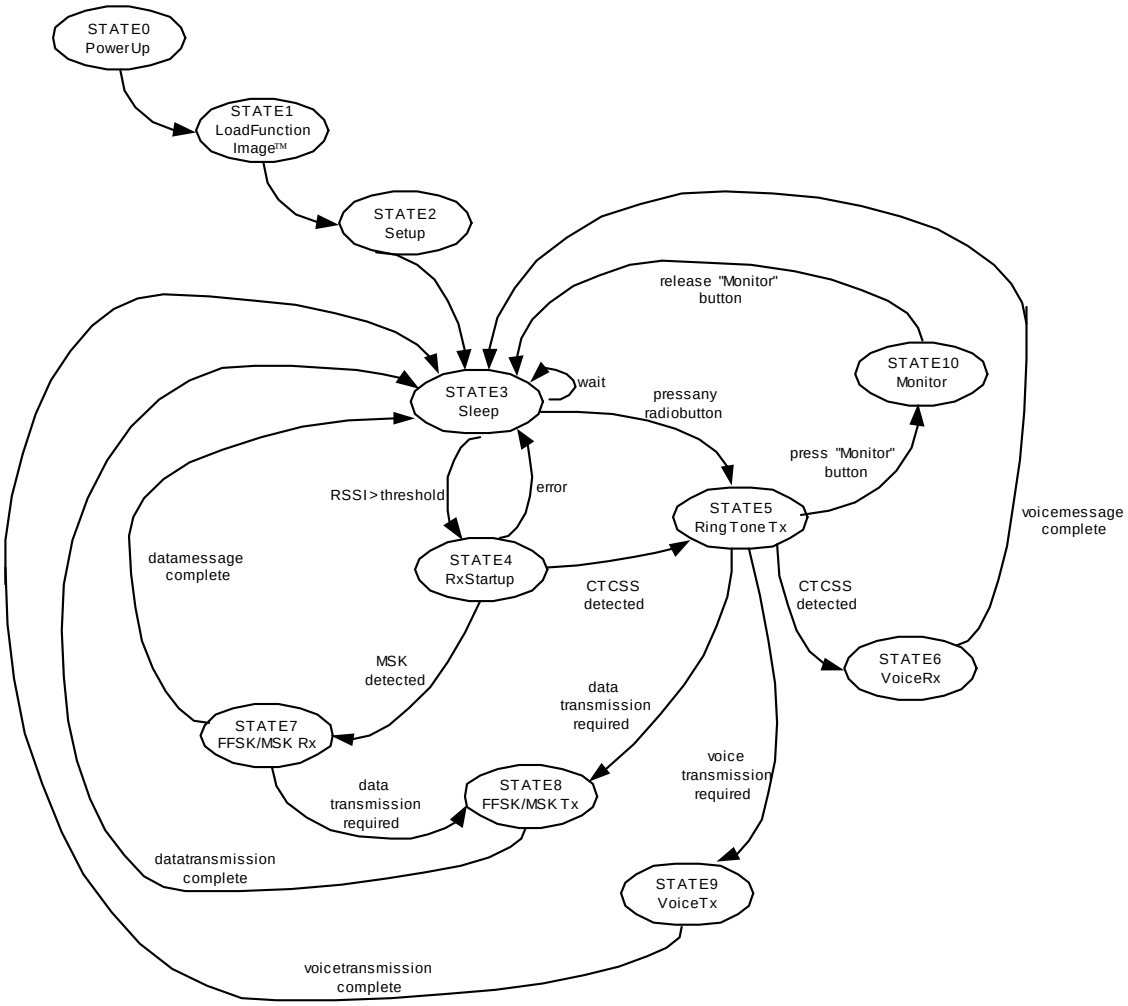

Figure 6: CMX7031 Application State Flow Diagram

5.1 STATE 0 and STATE 1: Initial States

STATE 0 involves the application of power to the CMX7031.

STATE 1, Load Function Image™, occurs after power is applied to the CMX7031. The Function Image™ loading procedure is discussed in Section 7.3 of the CMX7031 datasheet.

After the Function Image™ has been loaded, the CMX7031 will report back checksum values as well as its product identification code. The host microcontroller should verify that these values are correct. Once the verification is complete, the Function Image™ is activated by loading the CMX7031 with its 32-bit Device Activation Code.

The CMX7031 internal registers are now in the states described in Section 10.1.2 of the CMX7031 User Manual.

5.2 STATE 2: Setup

This state involves initial device configuration that will usually not have to be repeated during normal device operation. The functions performed in STATE 2 are as follows:

- System Clock Generator 1 = 12.288MHz for external components.
- System Clock Generator 2 = 16.384MHz for external components.
- RF Synthesizer Channel 1 = 462.5625MHz for Tx (FRS Channel 1).
- RF Synthesizer Channel 2 = 392.5625MHz for RF demodulator LO1 (FRS Channel 1).
- Audio signal processing blocks configured in preferred order.

The following table identifies the register manipulations implemented in STATE 2.

Register Address	Register Name	Register Contents	Effect
$AB	SYSTEM CLK 1 PLL	0x1200	SysClk1 VCO output divider = 4, SysClk1 PLL divider = 512
$AC	SYSTEM CLK 1 REF	0xE0C8	SysClk1 source = SysClk1 PLL, SysClk1 PLL enabled, normal O / P slew, reference divider = 200.
$AD	SYSTEM CLK 2 PLL	0x0E00	SysClk2 VCO output divider = 3, SysClk2 PLL divider = 512
$AE	SYSTEM CLK 2 REF	0xE0C8	SysClk2 source = SysClk2 PLL, SysClk2 PLL enabled, normal O / P slew, reference divider = 200.
$B2	RF CHANNEL DATA	0x408D	Channel 1 Tx configured for 462.5625MHz.
$B2	RF CHANNEL DATA	0x4424	
$B2	RF CHANNEL DATA	0x4A00	
$B2	RF CHANNEL DATA	0x4C01	
$B2	RF CHANNEL DATA	0x71BC	Channel 2 Rx configured for 392.5625MHz.
$B2	RF CHANNEL DATA	0x7405	
$B2	RF CHANNEL DATA	0x7A00	
$B2	RF CHANNEL DATA	0x7C01	
$C8	PROGRAMMING REGISTER (P1.0)	0xD6D6	Transmitted FFSK / MSK and ring tone level = 500mV$_{RMS}$.
$C8	PROGRAMMING REGISTER (P1.1)	0x50D9	50mV$_{RMS}$ FFSK / MSK detection threshold, inband detection bandwidth +/-1.3% (will decode).
$C8	PROGRAMMING REGISTER (P2.0)	0xE278	Transmitted CTCSS tone level = 45mV$_{RMS}$.
$C8	PROGRAMMING REGISTER (P2.1)	0x60B8	CTCSS detection threshold 25mV$_{RMS}$, CTCSS detection bandwidth +/-1.1% (will decode).
$C8	PROGRAMMING REGISTER (P2.2)	0x6000	Write to this register to access other Block 2 registers.
$C8	PROGRAMMING REGISTER (P2.3)	0x6000	
$C8	PROGRAMMING REGISTER (P2.4)	0x6000	
$C8	PROGRAMMING REGISTER (P2.5)	0x6F00	CTCSS drop out time = 120ms. (This represents the length of time the CTCSS tone can drop out before loss of CTCSS is asserted. The setting of this register also determines the deresponse time, which is typically 90ms longer than the programmed drop out time.)
$C8	PROGRAMMING REGISTER (P3.0)	0xF000	P3.0 = 0 (default ADC1 averaging length).
$C8	PROGRAMMING REGISTER (P3.1)	0x7000	P3.1 = 0 (default ADC2 averaging length).
$C8	PROGRAMMING REGISTER (P3.2)	0x7018	These writes configure the CMX7031 to use the 19.2MHz TCXO as its main clock source.
$C8	PROGRAMMING REGISTER (P3.3)	0x7099	
$C8	PROGRAMMING REGISTER (P3.4)	0x70C8	
$C8	PROGRAMMING REGISTER (P3.5)	0x7200	
$C8	PROGRAMMING REGISTER (P3.6)	0x7140	
$C8	PROGRAMMING REGISTER (P3.7)	0x7008	
$C8	PROGRAMMING REGISTER (P4.0)	0x8000	Write to this register to access other Block 4 registers.
$C8	PROGRAMMING REGISTER (P4.1)	0x0000	
$C8	PROGRAMMING REGISTER (P4.2)	0x0000	
$C8	PROGRAMMING REGISTER (P4.3)	0x0000	
$C8	PROGRAMMING REGISTER (P4.4)	0x0000	
$C8	PROGRAMMING REGISTER (P4.5)	0x0000	
$C8	PROGRAMMING REGISTER (P4.6)	0x0000	
$C8	PROGRAMMING REGISTER (P4.7)	0x1CB4	Tx Limiter set for limiting at 1.48V$_{PP}$ (525mV$_{RMS}$)
$C8	PROGRAMMING REGISTER (P4.8)	0x0000	Write to this register to access other Block 4 registers.
$C8	PROGRAMMING REGISTER (P4.9)	0x004B	Preferred order for audio signal processing blocks.
$A8	AUXDAC CONTROL / DATA	0x8974	DAC3 enabled and generating 1.2V signal for TCXO control signal.

Table 8: STATE 2 Register Settings

5.3 STATE 3: Sleep

This is the default operating state for the CMX7031 in this application.

In this condition, the CMX7031 is in idle mode and powered down to the maximum extent possible while monitoring for incoming carrier.

Highlights of STATE 3 are as follows:

- Channel 2 Synthesizer placed in Rx mode.
- DAC1 is disabled (this deactivates RAMDAC function used by Tx states).
- Received Signal Strength Indicator (RSSI) signal is monitored by ADC1 via AUXADC1 input pin.
- Battery voltage is monitored by ADC2 via AUXADC4 input pin.
- TCXO control signal provided on AUXDAC3 output pin.
- CMX7031 is powersaved to maximum extent possible.
- Device is placed into idle mode.

The following register configuration will achieve the previously stated objectives:

Register Address	Register Name	Register Contents	Effect
$B3	RF CHANNEL CONTROL	0x0500	RF synth clk = reference clk. Channel 2: 1 cycle phase lock tolerance, + charge polarity, low charge pump gain, Rx mode enabled. Channel 1: powersaved.
$A8	AUXDAC CONTROL / DATA	0x0000	Disable DAC1 (this is done because Tx states, which use DAC1's RAMDAC function, transition to this state once complete.)
$B5	AUXADC THRESHOLD	0x423E	ADC1 high threshold = 1.85V (RSSI high).
$B5	AUXADC THRESHOLD	0x0117	ADC1 low threshold = 0.9V (RSSI low).
$B5	AUXADC THRESHOLD	0xC1BE	ADC2 high threshold = 1.44V (corresponds to "low battery warning" of 3.6V).
$A7	AUXADC / TX MODE	0x07B0	ADC1 input from AUXADC1 input pin (RSSI), rolling averaging. ADC2 input from AUXADC4 input pin (battery voltage), rolling averaging. NOTE: Default averaging values in Program Block P3.0 and P3.1 result in 50% averaging.
$C0	POWER DOWN CONTROL	0x0050	Bias block enabled, Programming Register contents protected.
$CE	INTERRUPT MASK	0x8300	AUXADC1 and AUXADC2 IRQ enabled.
$C1	MODE CONTROL	0x0000	Idle mode.

Table 9: STATE 3 Register Settings

Possible subsequent states from STATE 3 include:

- STATE 4: RX Startup
  - This will occur if an incoming carrier signal causes the RSSI signal to exceed the ADC1 high threshold level.
- STATE 5: Ring Tone Tx
  - This will occur if the user presses a button on the radio.

5.4 STATE 4: RX Startup

In order to reach this state, incoming RF carrier has caused the RSSI signal to exceed the CMX7031's ADC1 high threshold. When this happens, STATUS Register ($C6) b8 = 1 and an IRQ is issued.

Two types of incoming signals are expected in this application scenario; voice and FFSK / MSK data. A voice call will be indicated by a CTCSS detection event, while incoming FFSK / MSK data will be marked by the absence of the CTCSS detection.

Highlights of STATE 4 include:

- Configure CMX7031 to receive signal from Disc input and pass signal through Input 1 to MSK and CTCSS detectors.
- Enable MSK and CTCSS detection.
- Enable receive audio processing circuits.

The CMX7031 is configured for receive operation as follows:

Register Address	Register Name	Register Contents	Effect
$B1	INPUT GAIN and OUTPUT SIGNAL ROUTING	0x0010	Input 1 and Input 2 = 0dB, Input 1 signal from Disc, MOD1 and MOD2 and Audio and Input 2 at bias.
$C0	POWER DOWN CONTROL	0x3050	Enabled: Disc amp, Input 1, bias block, xtal circuit. Programming Register contents protected.
$C2	AUDIO CONTROL	0x6CC9	Enabled: compandor, deemphasis, 25kHz filter, 300Hz HPF. CTCSS tone # 1 (67.0Hz) selected for receive.
$C7	MODEM CONTROL	0x00A0	Data packetizing mode, FFSK / MSK Mode 5 selected.
$CE	INTERRUPT MASK	0x8B72	Enabled IRQs: CTCSS, AUXADC1, AUXADC2, FFSK / MSK 2400 bps, RF status change
$C1	MODE CONTROL	0x0049	Subaudio source = Input 1, CTCSS enabled, FFSK / MSK source = Input 1, 2400 bps enabled, Rx mode.

Table 10: STATE 4 Register Settings

The CMX7031 will issue an interrupt once the incoming signal has been identified, and the STATUS register ($C6) can be read to determine the source of the interrupt. Expected interrupts include:

- $C6 b4 = 1: 2400 bps FFSK / MSK data has been received. Proceed to STATE 7, FFSK / MSK Rx.
- $C6 b11 = 1: a CTCSS tone has been received. Proceed to STATE 5, Ring Tone Tx (followed by STATE 6, Voice Rx).

Other interrupt sources indicate an error condition and should result in the firmware reverting to STATE 3 Sleep Mode.

5.5 STATE 5: Ring Tone Tx

The conditions that will result in reaching this state include:

- An incoming voice message has been detected.
- The user has pressed a button on the radio, such as “PTT”, “Poll”, or a keypad button while entering a text message.

The CMX7031 can be configured to generate audible tones for various purposes. The designer may wish to implement different alerting tones for different buttons. For example, the “PTT” button could generate one alerting tone, while the “Poll” button could generate a different alerting tone, and so on. This feature can allow the radio user to quickly determine which button has been pressed. Additionally, the CMX7031 can be configured to sequentially generate different tones, thereby creating simple melodies.

Audio tones can be generated by the CMX7031 in both Tx and Rx modes. Tones generated while in Tx mode are passed through the Tx Limiter, so Programming Block P4.7 (Tx Limiter Control) must be set to a nonzero value in order for an audio tone to come out of the CMX7031. The Tx Limiter does not affect audio tones generated in Rx mode.

The following register configurations will cause a ring tone of 1250Hz to be delivered to the external speaker driver. Other ring tones, as well as combinations of ring tones (i.e. melodies), are possible by loading different values into the AUDIO TONE ($CD) register.

Register Address	Register Name	Register Contents	Effect
$CD	AUDIO TONE	0x04E2	Loads 1250Hz tone for generation.
$B1	INPUT GAIN AND OUTPUT SIGNAL ROUTING	0x0040	Audio output = Output 1 signal
$B0	ANALOGUE OUTPUT GAIN	0x000F	Audio output attenuation = 0dB.
$A7	AUXADC / TX MODE	0x17B0	Output 1 = Inband tones, ADC1 input from AUXADC1 input pin (RSSI), rolling averaging. ADC2 input from AUXADC4 input pin (battery voltage), rolling averaging. NOTE: Default averaging values in Program Block P3.0 and P3.1 result in 50% averaging.
$C0	POWER DOWN CONTROL	0x08D0	Enabled: Output 1, Audio Output, Bias block, crystal oscillator circuit. Programming Register contents protected
$CE	INTERRUPT MASK	0x8200	Enabled IRQ: AUXADC2 (battery voltage monitoring).
$C1	MODE CONTROL	0x0402	Inband processing mode = Audio Tones, Tx mode.

Table 11: STATE 5 Register Settings

Once the above steps have been performed, all that is required to generate a different tone is to load a different value into the AUDIO TONE (0xCD) Register. This feature can allow simple melodies to be played over the radio’s speaker.

Once the desired ring tone generation is complete, the CMX7031 software should move to one of the following states as needed:

- STATE 6 Voice Rx
- STATE 8 FFSK / MSK Tx
- STATE 9 Voice Tx
- STATE 10 Monitor

5.6 STATE 6: Voice Rx

At this point, the CMX7031 has detected a CTCSS tone that matches the CTCSS address programmed into the AUDIO CONTROL ($C2) register. This means that the incoming transmission is a voice call intended for the radio's user. The following register manipulations will configure the CMX7031 to process the incoming voice call and present it to the Audio Output pin.

Register Address	Register Name	Register Contents	Effect
$B1	INPUT GAIN and OUTPUT SIGNAL ROUTING	0x0050	Input 1 gain = 0dB, Input 1 source = Disc, Audio Output = Output 1 (Rx signal processing path).
$C0	POWER DOWN CONTROL	0x38D0	Enabled: Disc amp, Input 1, Output 1, Audio output, Bias block, crystal oscillator circuit. Programming Register contents protected.
$B0	ANALOGUE OUTPUT GAIN	0x000F	Audio output attenuation = 0dB.
$CE	INTERRUPT MASK	0x8B02	Enabled interrupts: CTCSS, AUXADC1, AUXADC2, RF status change.
$C1	MODE CONTROL	0x4041	Audio source = Input 1, audio processing path enabled, subaudio source = Input 1, CTCSS detection enabled, Rx mode.

Table 12: STATE 6 Register Settings

5.7 STATE 7: FFSK / MSK Rx

At this point, the CMX7031 has detected the presence of RF carrier and 2400 bps FFSK / MSK signals. The CMX7031 is configured to receive this FFSK / MSK message as follows:

Register Address	Register Name	Register Contents	Effect
$B6	MODEM ADDRESS	0x4F00	Address 79d programmed.
$CE	INTERRUPT MASK	0x83F2	Enabled interrupts: AUXADC1, AUXADC2, FFSK / MSK data complete, data ready, data CRC, 2400 bps, RF status change.
$C1	MODE CONTROL	0x0009	Subaudio source = Input 1, FFSK / MSK source = Input 1, 2400 bps enabled, Rx mode.

Table 13: STATE 7 Register Settings

A timer should be started to prevent the CMX7031 from continuously searching for a Frame Head should an error condition occur.

The CMX7031 will check the incoming Frame Head for a valid Checksum A, and if found, will then compare the address in Control Field byte 1 to the user programmed address in the Modem Address ($B6) register. (The CMX7031 will also check for a "40" FFSK / MSK address.) The CMX7031 will set b5 of the Status register and issue an interrupt if Checksum A indicates correct Frame Head bytes and if the FFSK / MSK addresses match. The host microcontroller can read out the address and size / information bytes from Rx Data # 1 register ($C5), and optionally, the Control byte and Frame Head Checksum A byte from Rx Data # 2 register ($C9).

The CMX7031 will then issue interrupts when new data is ready for host processing. The four available received data bytes can be read out of Rx Data # 1 and # 2 ($C5 and $C9) registers. The host microcontroller has approximately 20ms to read out the new data after the interrupt has been issued; otherwise, new incoming data will overwrite the old data.

Status register ($C6) b7,6 = 11 when the last byte of the data frame has been received. When b7 = 1 is detected, the firmware should revert to STATE 3, Sleep.

5.8 STATE 8: FFSK / MSK Tx

To reach this state, data transmission is required. Since either STATE 5 (Ring Tone Tx) or STATE 7 (FFSK / MSK Rx) can transition to this state, additional register manipulations must be performed to ensure that the device is properly configured.

Highlights of this state include:

- Switch Channel 1 Synthesizer to its "Tx" setting.
- Configure modem for Type 5 message format at 2400 bps.
- Configure signal paths to allow MSK signal to be presented at MOD1 output.
- Activate DAC2 so it can supply Tx PA with temperature compensation signal.
- Enable DAC1 as a RAMDAC to create a smooth transmit ramp profile.

The "Type 5" FFSK / MSK message format has been selected for this application. With this format, the host is responsible for loading the "Address" and "Size" bytes for transmission. Once this is done, the CMX7031 will add the "Format" byte and all necessary formatting information.

FFSK / MSK data transfer is initiated with the following commands:

REGISTER ADDRESS	REGISTER NAME	REG CONTENTS	EFFECT
$C1	MODE CONTROL	0x0000	Idle mode.
$B3	RF CHANNEL CONTROL	0x0003	Channel 1 Synthesizer enabled and set to Tx, Channel 2 Synthesizer powersaved.
$CA	TX DATA	0x1E14	Address = 0x1E (30d), size = 0x14 (20d).
$C7	MODEM CONTROL	0x00A0	Data packetizing enabled, Type 5 message format, standard scrambling seed. (Note that bit 2, "User Data", is not used in this application.)
$A7	AUXADC / TX MODE	0x1734	Output 1 = Inband, ADC2 input from AUXADC3 input pin (TCXO temperature) with rolling averaging. ADC1 input from AUXADC2 input pin (Tx PA temperature) with rolling averaging. NOTE: Default averaging values in Program Block P3.0 and P3.1 result in 50% averaging.
$A8	AUXDAC CONTROL / DATA	0x8574	DAC2 enabled and generating 1.2V signal (value arbitrarily chosen) for Tx PA temperature compensation signal. (DAC3, used for TCXO temperature compensation, is already running after being configured in STATE 3.)
$B0	ANALOGUE OUTPUT GAIN	0x7000	MOD1 = 0dB.
$B1	INPUT GAIN AND OUTPUT SIGNAL ROUTING	0x0200	MOD1 source = Output 1.
$C0	POWER DOWN CONTROL	0x0A50	Enabled: Output 1, MOD1, Bias block, crystal oscillator circuit. Programming Register contents protected.
$CE	INTERRUPT MASK	0x83C2	Enabled: AUXADC2, AUXADC1, FFSK / MSK transmission end, FFSK / MSK data transfer required, RF status change.
$A8	AUXDAC CONTROL / DATA	0x9005	RAMDAC ramp up started.
$C1	MODE CONTROL	0x000A	2400 bps FFSK / MSK enabled, Tx mode.

Table 14: STATE 8 Register Settings

The CMX7031 will issue interrupts when additional Tx data is required. Once a "data transfer required" interrupt is received, the host must load new data before the current data has been transmitted; otherwise, the current data will be retransmitted. Subsequent FFSK / MSK data bytes should be written to $CA and $CB; the Tx data buffer is four bytes deep for Type 5 message format. The data to be loaded into $CA and $CB must be loaded with separate C-BUS transactions (i.e. one C-BUS transaction for $CA data, and another C-BUS transaction for $CB data).

When the final bit of FFSK / MSK data has been transmitted, an IRQ will be generated with STATUS Register ($C6) b7 = 1. This event indicates the conclusion of the FFSK / MSK transmission. The CMX7031 can now be powersaved by returning to STATE 3.

5.9 STATE 9: Voice Tx

To reach this point, the CMX7031 has transitioned from the Sleep state (STATE 3) and the Ring Tone Tx state (STATE 5).

Highlights of this state include:

- Switch Channel 1 Synthesizer to its “Tx” setting.
- Enable and configure audio processing circuits.
- Configure signal paths to allow voice signal and CTCSS signal to be summed and presented at MOD1 output.
- Activate DAC2 so it can supply Tx PA with temperature compensation signal.
- Enable DAC1 as a RAMDAC to create a smooth transmit ramp profile.

The following register configurations will make voice transmission possible:

Register Address	Register Name	Register Contents	Effect
$C1	MODE CONTROL	0x0000	Idle mode
$B3	RF CHANNEL CONTROL	0x0003	Channel 1 Synthesizer switched to Tx, Channel 2 Synthesizer powersaved.
$A7	AUXADC / TX MODE	0x2734	Output 1 = Inband + subaudio, ADC2 input from AUXADC3 input pin (TCXO temperature) with rolling averaging. ADC1 input from AUXADC2 input pin (Tx PA temperature) with rolling averaging. NOTE: Default averaging values in Program Block P3.0 and P3.1 result in 50% averaging.
$A8	AUXDAC CONTROL / DATA	0x8574	DAC2 enabled and generating 1.2V signal (value arbitrarily chosen) for Tx PA temperature compensation signal. (DAC3, used for TCXO temperature compensation, is already running after being configured in STATE 3.)
$B0	ANALOGUE OUTPUT GAIN	0x7000	MOD1 = 0dB.
$B1	INPUT GAIN AND OUTPUT SIGNAL ROUTING	0x0230	Input 1 = 0dB, MOD1 = Output 1 (inband and subaudio signals), Input 1 routing = mic.
$C0	POWER DOWN CONTROL	0x5A50	Enabled: Mic amp, Input 1, Output 1, MOD1, Bias block, crystal oscillator circuit. Programming Register contents protected.
$C2	AUDIO CONTROL	0x68DC	Companding enabled, preemphasis enabled, 25.0kHz channel filtering, CTCSS tone # 20 selected.
$CE	INTERRUPT MASK	0x8302	Enabled IRQs: AUXADC2, AUXADC1, RF status change.
$A8	AUXDAC CONTROL / DATA	0x9005	RAMDAC ramp up started.
$C1	MODE CONTROL	0x4042	Audio processing path enabled, CTCSS enabled, Tx mode.

Table 15: STATE 9 Register Settings

Once these steps are complete, processed voice and a 67.0Hz CTCSS subaudio tone (address #1) will be transmitted from the MOD1 output.

When the user releases the “Push To Talk” button, the transmit phase is complete. A value of 0x9001 can be written to the AuxDAC CONTROL / DATA register to allow for a Tx PA ramp down, if desired. The CMX7031 software should then migrate back to STATE 3, Sleep.

5.10 STATE 10: Monitor

In certain situations, such as reception at the fringe of the coverage area, the radio user may wish to listen to all activity on a channel. This “monitor” mode can be performed at any time but would most likely be performed while the radio is in STATE 3, Sleep.

Activating a “monitor” mode can be done easily by configuring the CMX7031 as follows. Please note that the Channel 2 Synthesizer, used for Rx LO1 generation, is already enabled because of action in STATE 3, “Sleep”.

Register Address	Register Name	Register Contents	Effect
$C1	MODE CONTROL	0x0000	Idle mode
$B0	ANALOGUE OUTPUT GAIN	0x000F	Audio output attenuation = 0dB.
$B1	INPUT GAIN and OUTPUT SIGNAL ROUTING	0x0050	Input 1 = Disc, Audio Output = Output 1 (Rx signal processing path).
$C0	POWER DOWN CONTROL	0x38D0	Enabled: Disc amp, Input 1, Output 1, Audio output, Bias block, crystal oscillator circuit. Programming Register contents protected.
$C2	AUDIO CONTROL	0x6C00	Enabled: compandor, deemphasis, 25kHz filter, 300Hz HPF.
$CE	INTERRUPT MASK	0x8202	Enabled interrupts: AUXADC 2, RF status change.
$C1	MODE CONTROL	0x4001	Audio source = Input 1, audio processing path enabled, Rx mode.

Table 16: STATE 10 Register Settings

The CMX7031 will now pass all recovered signals to the external speaker driver amplifier. When the channel monitoring is complete, the CMX7031 can be powersaved by moving back to STATE 3.

6 Conclusion

FRS type radios are very common in today’s marketplace, and innovative features such as text messaging and the ability to display location information is key for product differentiation and market success.

The CMX7031 is a feature rich baseband processor that enables innovative features while allowing low power consumption and small form factor end products. The purpose of this document was to illustrate how the CMX7031 can be configured to perform such features in a real application. It is hoped that this document will assist the designer in developing exciting new products based on the CMX7031.

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